

WHAT IS CLAIMED IS:

1 1. A method for testing memory of an information handling system, the
2 method comprising:

3 initiating startup of the information handling system;
4 determining that a memory test is required;
5 generating test data according to one or more test routines with the
6 information handling system CPU, the CPU having SIMD registers;
7 communicating the test data to and from a predetermined portion of the
8 memory through the SIMD registers; and
9 passing the memory test if test data communicated from the memory has a
10 predetermined relationship with the generated test data.

1 2. The method of Claim 1 further comprising:

2 using CPU 64-bit MMX registers for temporary storage of the test data.

1 3. The method of Claim 1 wherein the predetermined portion comprises
2 at least one Mbyte, the method further comprising:

3 incrementing the memory address of the predetermined portion by the at least
4 one Mbyte;
5 repeating the generating, communicating and passing for the incremented
6 portion of memory; and
7 repeating the incrementing until each portion of the memory passed the
8 memory test.

1 4. The method of Claim 3 wherein determining an memory test is
2 required further comprises setting the gate A20 to support the memory test before the
3 generating of test data, the method further comprising:

4 maintaining the gate A20 setting through each incrementing; and
5 resetting the gate A20 after each portion of the memory passes the memory
6 test.

1 5. The method of Claim 3 wherein determining a memory test is required
2 further comprises entering the protected mode before the generating of test data, the
3 method further comprising:

4 maintaining the protected mode through each incrementing; and
5 exiting the protected mode after each portion of the memory passes the
6 memory test.

1 6. The method of Claim 1 wherein generating the test data further
2 comprises:

3 using ADD and SUB instructions; and
4 avoiding INC and DEC instructions.

1 7. The method of Claim 6 wherein generating the test data further
2 comprises:

3 generating test data with a boundary test routine; and
4 generating test data with a stuck bit test routine.

1 8. The method of Claim 7 wherein generating test data further comprises
2 executing 32-bit code on the CPU.

1 9. The method of Claim 1 wherein generating test data further comprises:
2 using the MOVNTDQ instruction on the CPU to move test data in the memory
3 in 128-bit increments.

1 10. An information handling system comprising:
2 a CPU operable to perform instructions;
3 random access memory interfaced with the CPU and operable to store
4 information;
5 a firmware operable to startup the CPU to an operational state, the firmware
6 further operable to coordinate execution of instructions by the CPU to
7 test the memory, the instructions comprising 32-bit code to:
8 initiate a memory test during startup;

9 generate test data to write to and read from the random access memory using
10 128-bit SIMD registers and the MOVNTDQ instruction;
11 apply the test data iteratively to predetermined sized portions of the random
12 access memory until the test data has been written to and read from
13 each portion; and
14 passing the memory test if test data read from the random access memory has
15 a predetermined relationship with the test data written to the random
16 access memory.

1 11. The information handling system of Claim 10 wherein the instructions
2 to generate test data further comprise instructions to:
3 perform a walking 1s and 0s routine; and
4 perform a multi-pattern routine.

1 12. The information handling system of Claim 11 wherein the instructions
2 to generate test data comprise ADD and SUB instructions and lack INC and DEC
3 instructions.

1 13. The information handling system of Claim 12 wherein the portions are
2 at least one Mbyte in size.

1 14. The information handling system of Claim 10 further comprising
2 instructions to:
3 set gate A20 before generating the test data;
4 maintain the gate A20 setting through each iterative application of the test data
5 to the portions; and
6 reset gate A20 upon completion of all iterative applications of the test data.

1 15. The information handling system of Claim 10 further comprising
2 instructions to:
3 enter a protected mode before generating the test data;
4 maintain the protected mode through each iterative application of the test data
5 to the portions; and

6 exiting the protected mode upon completion of all iterative applications of the
7 test data.

1 16. The information handling system of Claim 10 further comprising
2 instructions to use 64-bit MMX registers of the CPU for temporary storage of test
3 data.

1 17. A method for testing memory at boot of an information handling
2 system, the method comprising:

3 initiating a memory test during POST;
4 generating test data to write to and read from the memory using 128-bit SIMD
5 registers and the MOVNTDQ instruction;
6 applying the test data iteratively to predetermined sized portions of the
7 memory until the test data has been written to and read from each
8 portion; and
9 passing the memory test if test data read from the random access memory has
10 a predetermined relationship with the test data written to the random
11 access memory.

1 18. The method of Claim 17 further comprising:
2 setting gate A20 and entering the protected mode before generating the test
3 data;
4 maintaining the gate A20 setting and protected mode through each iterative
5 application of the test data to the portions; and
6 resetting gate A20 and exiting the protective mode upon completion of the
7 iterative applications of the test data to each portion of the memory.

- 1 19. The method of Claim 18 wherein generating test data further
- 2 comprises:
 - 3 executing a walking 1s and 0s test routine; and
 - 4 executing a multi-pattern test routine.

1 20. The method of Claim 19 wherein generating test data further comprises
2 executing ADD and SUB instructions.